

Department of Electronics & Communication

Digital Electronics

Part - A

Unit – 1

## 1. Define binary logic?

Binary logic consists of binary variables and logical operations. The variables are designated by the alphabets such as A, B, C, x, y, z, etc., with each variable having only two distinct values: 1 and 0. There are three basic logic operations: AND, OR, and NOT.

## 2. What are the basic digital logic gates?

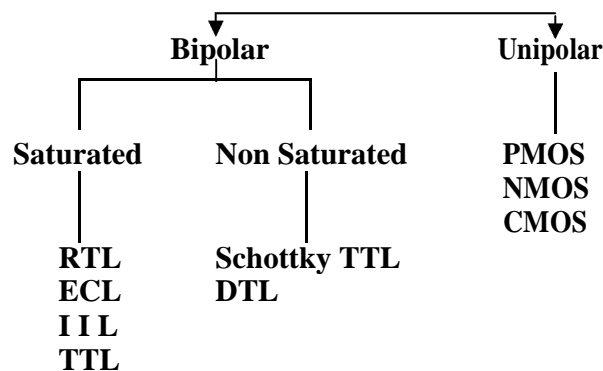
The three basic logic gates are

AND gate  
OR gate  
NOT gate

## 3. What is a Logic gate?

Logic gates are the basic elements that make up a digital system. The electronic gate is a circuit that is able to operate on a number of binary inputs in order to perform a particular logical function.

## 4. Give the classification of logic families



## 5. Which gates are called as the universal gates? What are its advantages?

The NAND and NOR gates are called as the universal gates. These gates are used to perform any type of logic application.

## 6. Classify the logic family by operation?

The Bipolar logic family is classified into

Saturated logic

Unsaturated logic.

The RTL, DTL, TTL, I<sup>2</sup>L, HTL logic comes under the saturated logic family.

The Schottky TTL, and ECL logic comes under the unsaturated logic family.

7. State the classifications of FET devices. FET is classified as

1. Junction Field Effect Transistor (JFET)

2. Metal oxide semiconductor family (MOS).

8. Mention the classification of saturated bipolar logic families.

The bipolar logic family is classified as follows:

RTL- Resistor Transistor Logic

DTL- Diode Transistor logic I<sup>2</sup>L-

Integrated Injection Logic TTL-

Transistor Transistor Logic

ECL- Emitter Coupled Logic

9. Mention the important characteristics of digital IC's? Fan out

Power dissipation

Propagation Delay

Noise Margin

Fan In

Operating temperature

Power supply requirements

10. Define Fan-out?

Fan out specifies the number of standard loads that the output of the gate can drive with out impairment of its normal operation.

11. Define power dissipation?

Power dissipation is measure of power consumed by the gate when fully driven by all its inputs.

12. What is propagation delay?

Propagation delay is the average transition delay time for the signal to propagate from input to output when the signals change in value. It is expressed in ns.

13. Define noise margin?

It is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in the circuit output. It is expressed in volts.

14. Define fan in?

Fan in is the number of inputs connected to the gate without any degradation in the voltage level.

**15. What is Operating temperature?**

All the gates or semiconductor devices are temperature sensitive in nature. The temperature in which the performance of the IC is effective is called as operating temperature. Operating temperature of the IC vary from  $0^{\circ}\text{C}$  to  $70^{\circ}\text{C}$ .

**16. What is High Threshold Logic?**

Some digital circuits operate in environments, which produce very high noise signals. For operation in such surroundings there is available a type of DTL gate which possesses a high threshold to noise immunity. This type of gate is called HTL logic or High Threshold Logic.

**17. What are the types of TTL logic?**

1. Open collector output
2. Totem-Pole Output
3. Tri-state output.

**18. What is depletion mode operation MOS?**

If the channel is initially doped lightly with p-type impurity a conducting channel exists at zero gate voltage and the device is said to operate in depletion mode.

**19. What is enhancement mode operation of MOS?**

If the region beneath the gate is left initially uncharged the gate field must induce a channel before current can flow. Thus the gate voltage enhances the channel current and such a device is said to operate in the enhancement mode.

**20. Mention the characteristics of MOS transistor?**

1. The n- channel MOS conducts when its gate- to- source voltage is positive.
2. The p- channel MOS conducts when its gate- to- source voltage is negative
3. Either type of device is turned off if its gate- to- source voltage is zero.

**21. How schottky transistors are formed and state its use?**

A schottky diode is formed by the combination of metal and semiconductor. The presence of schottky diode between the base and the collector prevents the transistor from going into saturation. The resulting transistor is called as schottky transistor.

The use of schottky transistor in TTL decreases the propagation delay without a sacrifice of power dissipation.

**22. List the different versions of TTL**

- |                         |                        |
|-------------------------|------------------------|
| 1.TTL (Std.TTL)         | 2.LTTL (Low Power TTL) |
| 3.HTTL (High Speed TTL) | 4.STTL (Schottky TTL)  |

**5.LSTTL (Low power Schottky TTL)**

**23. Why totem pole outputs cannot be connected together.**

Totem pole outputs cannot be connected together because such a connection might produce excessive current and may result in damage to the devices.

**24. State advantages and disadvantages of TTL Adv:**

Easily compatible with other ICs  
Low output impedance

**Disadv:**

Wired output capability is possible only with tristate and open collector types  
Special circuits in Circuit layout and system design are required.

**25. When does the noise margin allow digital circuits to function properly.**

When noise voltages are within the limits of  $V_{NA}$  (High State Noise Margin) and  $V_{NK}$  for a particular logic family.

**26. What happens to output when a tristate circuit is selected for high impedance.**

Output is disconnected from rest of the circuits by internal circuitry.

**27. What is 14000 series.**

It is the oldest and standard CMOS family. The devices are not pin compatible or electrically compatible with any TTL Series.

Unit – II

**28. Define combinational logic**

When logic gates are connected together to produce a specified output for certain specified combinations of input variables, with no storage involved, the resulting circuit is called combinational logic.

**29. Explain the design procedure for combinational circuits The problem definition**

Determine the number of available input variables & required O/P variables. Assigning letter symbols to I/O variables

Obtain simplified Boolean expression for each O/P. Obtain the logic diagram.

**30. Define Half adder and full adder**

The logic circuit that performs the addition of two bits is a half adder. The

circuit that performs the addition of three bits is a full adder.

**31. Define Decoder?**

A decoder is a multiple - input multiple output logic circuit that converts coded inputs into coded outputs where the input and output codes are different.

**32. What is binary decoder?**

A decoder is a combinational circuit that converts binary information from n input lines to a maximum of  $2^n$  out puts lines.

**33. Define Encoder?**

An encoder has  $2^n$  input lines and n output lines. In encoder the output lines generate the binary code corresponding to the input value.

**34. What is priority Encoder?**

A priority encoder is an encoder circuit that includes the priority function. In priority encoder, if 2 or more inputs are equal to 1 at the same time, the input having the highest priority will take precedence.

**35. Define multiplexer?**

Multiplexer is a digital switch. It allows digital information from several sources to be routed onto a single output line.

**36. What do you mean by comparator**

A comparator is a special combinational circuit designed primarily to compare the relative magnitude of two binary numbers.

### Unit 3

**37. List basic types of programmable logic devices.**

- . Read only memory
- . Programmable logic Array
- . Programmable Array Logic

**38. Explain ROM**

A read only memory(ROM) is a device that includes both the decoder and the OR gates within a single IC package. It consists of n input lines and m output lines. Each bit combination of the input variables is called an address. Each bit combination that comes out of the output lines is called a word. The number of distinct addresses possible with n input variables is  $2^n$ .

**39. Define address and word:**

In a ROM, each bit combination of the input variable is called an address. Each bit combination that comes out of the output lines is called a word.

40. State the types of ROM

- . Masked ROM.
- . Programmable Read only Memory
- . Erasable Programmable Read only memory.
- . Electrically Erasable Programmable Read only Memory.

41. What is programmable logic array? How it differs from ROM?

In some cases the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a PLA. A PLA is similar to a ROM in concept; however it does not provide full decoding of the variables and does not generate all the minterms as in the ROM.

42. Which gate is equal to AND-invert Gate? NAND gate.

43. Which gate is equal to OR-invert Gate? NOR gate.

44. Bubbled OR gate is equal to-----  
NAND gate

45. Bubbled AND gate is equal to-----  
NOR gate

46. Explain PROM.

**PROM (Programmable Read Only Memory)**

It allows user to store data or program. PROMs use the fuses with material like nichrome and polycrystalline. The user can blow these fuses by passing around 20 to 50 mA of current for the period 5 to 20 $\mu$ s. The blowing of fuses is called programming of ROM. The PROMs are one time programmable. Once programmed, the information is stored permanent.

47. Explain EPROM.

**EPROM (Erasable Programmable Read Only Memory)**

EPROM use MOS circuitry. They store 1's and 0's as a packet of charge in a buried layer of the IC chip. We can erase the stored data in the EPROMs by exposing the chip to ultraviolet light via its quartz window for 15 to 20 minutes. It is not possible to erase selective information. The chip can be reprogrammed.

48. Explain EEPROM.

**EEPROM (Electrically Erasable Programmable Read Only Memory)**

EEPROM also use MOS circuitry. Data is stored as charge or no charge on an insulated layer or an insulated floating gate in the device. EEPROM allows selective erasing at the register level rather than erasing all the information since the information can be changed by using electrical signals.

**49. What is RAM?**

**Random Access Memory. Read and write operations can be carried out.**

**50. What is programmable logic array? How it differs from ROM?**

**In some cases the number of don't care conditions is excessive, it is more economical to use a second type of LSI component called a PLA. A PLA is similar to a ROM in concept; however it does not provide full decoding of the variables and does not generate all the minterms as in the ROM.**

**51. What is mask-programmable?**

**With a mask-programmable PLA, the user must submit a PLA program table to the manufacturer.**

**52. What is field-programmable logic array?**

**The second type of PLA is called a field-programmable logic array. The user by means of certain recommended procedures can program the EPLA.**

**53. List the major differences between PLA and PAL**

**PLA:**  
**Both AND and OR arrays are programmable and Complex Costlier than PAL**

**PAL**  
**AND arrays are programmable OR arrays are fixed Cheaper and Simpler**

**54. Define PLD.**

**Programmable Logic Devices consist of a large array of AND gates and OR gates that can be programmed to achieve specific logic functions.**

**55. Give the classification of PLDs.**

**PLDs are classified as PROM(Programmable Read Only Memory), Programmable Logic Array(PLA), Programmable Array Logic (PAL), and Generic Array Logic(GAL)**

**56. Define PROM.**

**PROM is Programmable Read Only Memory. It consists of a set of fixed AND gates connected to a decoder and a programmable OR array.**

**57. Define PLA**

**PLA is Programmable Logic Array(PLA). The PLA is a PLD that consists of a programmable AND array and a programmable OR array.**

## 58. Define PAL

**PAL is Programmable Array Logic. PAL consists of a programmable AND array and a fixed OR array with output logic.**

## 59. Why was PAL developed ?

**It is a PLD that was developed to overcome certain disadvantages of PLA, such as longer delays due to additional fusible links that result from using two programmable arrays and more circuit complexity.**

## 60. Why the input variables to a PAL are buffered

**The input variables to a PAL are buffered to prevent loading by the large number of AND gate inputs to which available or its complement can be connected.**

## 61. What does PAL 10L8 specify ?

**PAL - Programmable Logic Array  
10 - Ten inputs  
L - Active LOW Output  
8 - Eight Outputs**

## 62. Give the comparison between PROM and PLA.

### **PROM**

- 1. And array is fixed and OR array is programmable.**
- 2. Cheaper and simple to use.**

### **PLA**

**Both AND and OR arrays are Programmable.  
Costliest and complex than PROMS.**

## Unit 4

## 63. What are the classification of sequential circuits?

**The sequential circuits are classified on the basis of timing of their signals into two types. They are,**

- 1) Synchronous sequential circuit.**
- 2) Asynchronous sequential circuit.**

**64. Define Flip flop.**

The basic unit for storage is flip flop. A flip-flop maintains its output state either at 1 or 0 until directed by an input signal to change its state.

**65. What are the different types of flip-flop?**

There are various types of flip flops. Some of them are mentioned below they are, ùRS flip-flop

ùSR flip-flop

ùD flip-flop

ùJK flip-flop

ùT flip-flop

**66. What is the operation of D flip-flop?**

In D flip-flop during the occurrence of clock pulse if  $D=1$ , the output Q is set and if  $D=0$ , the output is reset.

**67. What is the operation of JK flip-flop?**

- When K input is low and J input is high the Q output of flip-flop is set.
- When K input is high and J input is low the Q output of flip-flop is reset.
- When both the inputs K and J are low the output does not change
- When both the inputs K and J are high it is possible to set or reset the flip-flop (ie) the output toggle on the next positive clock edge.

**68. What is the operation of T flip-flop?**

T flip-flop is also known as Toggle flip-flop.

- When  $T=0$  there is no change in the output.
- When  $T=1$  the output switch to the complement state (ie) the output toggles.

**69. Define race around condition.**

In JK flip-flop output is fed back to the input. Therefore change in the output results change in the input. Due to this in the positive half of the clock pulse if both J and K are high then output toggles continuously. This condition is called 'race around condition'.

**70. What is edge-triggered flip-flop?**

The problem of race around condition can be solved by edge triggering flip flop. The term edge triggering means that the flip-flop changes state either at the positive edge or negative edge of the clock pulse and it is sensitive to its inputs only at this transition of the clock.

**71. What is a master-slave flip-flop?**

A master-slave flip-flop consists of two flip-flops where one circuit serves as a

master and the other as a slave.

**72. Define rise time.**

The time required to change the voltage level from 10% to 90% is known as rise time( $t_r$ ).

**73. Define fall time.**

The time required to change the voltage level from 90% to 10% is known as fall time( $t_f$ ).

**74. Define skew and clock skew.**

The phase shift between the rectangular clock waveforms is referred to as skew and the time delay between the two clock pulses is called clock skew.

**75. Define setup time.**

The setup time is the minimum time required to maintain a constant voltage levels at the excitation inputs of the flip-flop device prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as  $t_{setup}$ .

**76. Define hold time.**

The hold time is the minimum time for which the voltage levels at the excitation inputs must remain constant after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. It is denoted as  $t_{hold}$ .

**77. Define propagation delay.**

A propagation delay is the time required to change the output after the application of the input.

**78. Define registers.**

A register is a group of flip-flops flip-flop can store one bit information. So an n-bit register has a group of n flip-flops and is capable of storing any binary information/number containing n-bits.

**79. Define shift registers.**

The binary information in a register can be moved from stage to stage within the register or into or out of the register upon application of clock pulses. This type of bit movement or shifting is essential for certain arithmetic and logic operations used in microprocessors. This gives rise to group of registers called shift registers.

**80. What are the different types of shift type?**

There are five types. They are,

- ùSerial In Serial Out Shift Register
- ùSerial In Parallel Out Shift Register
- ùParallel In Serial Out Shift Register
- ùParallel In Parallel Out Shift Register

ùBidirectional Shift Register

81. Explain the flip-flop excitation tables for RS

FF. RS flip-flop

In RS flip-flop there are four possible transitions from the present state to the next state. They are,

- 0 0 transition:** This can happen either when  $R=S=0$  or when  $R=1$  and  $S=0$ .
- 0 1 transition:** This can happen only when  $S=1$  and  $R=0$ .
- 1 0 transition:** This can happen only when  $S=0$  and  $R=1$ .

**1 1 transition:** This can happen either when  $S=1$  and  $R=0$  or  $S=0$  and  $R=0$ .

82. Define sequential circuit?

In sequential circuits the output variables dependent not only on the present input variables but they also depend up on the past history of these input variables.

83. Give the comparison between combinational circuits and sequential circuits.

Combinational circuits	Sequential circuits
Memory unit is not required	Memory unity is required
Parallel adder is a combinational circuit	Serial adder is a sequential circuit

84. What do you mean by present state?

The information stored in the memory elements at any given time define.s the present state of the sequential circuit.

85. What do you mean by next state?

The present state and the external inputs determine the outputs and the next state of the sequential circuit.

86. State the types of sequential circuits?

1. Synchronous sequential circuits
2. Asynchronous sequential circuits

87. Define synchronous sequential circuit

In synchronous sequential circuits, signals can affect the memory elements only at discrete instant of time.

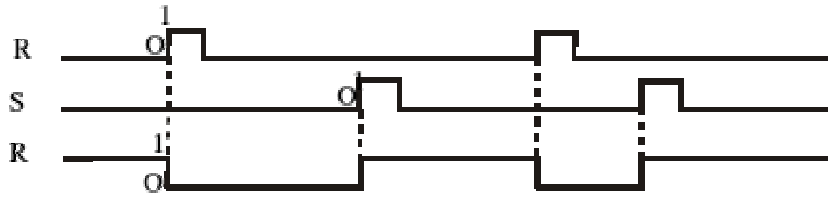
Unit 5

88. Define Asynchronous sequential circuit?

In asynchronous sequential circuits change in input signals can affect memory element at any instant of time.

**89. Give the comparison between synchronous & Asynchronous sequential circuits?**

<b>Synchronous sequential circuits</b>	<b>Asynchronous sequential circuits.</b>
<b>Memory elements are clocked flip-flops</b>	<b>Memory elements are either unlocked flip - flops or time delay elements.</b>
<b>Easier to design</b>	<b>More difficult to design</b>



90. The following wave forms are applied to the inputs of SR latch. Determine the Q waveform Assume initially Q = 1

Here the latch input has to be pulsed momentarily to cause a change in the latch output state, and the output will remain in that new state even after the input pulse is over.

91. What is race around condition?

In the JK latch, the output is feedback to the input, and therefore changes in the output results change in the input. Due to this in the positive half of the clock pulse if J and K are both high then output toggles continuously. This condition is known as race around condition.

92. Give the comparison between synchronous & Asynchronous counters.

Asynchronous counters	Synchronous counters
In this type of counter flip-flops are connected in such a way that output of 1st flip-flop drives the clock for the next flip-flop.	In this type there is no connection between output of first flip-flop and clock input of the next flip - flop
All the flip-flops are Not clocked simultaneously	All the flip-flops are clocked simultaneously

93. The  $t_{pd}$  for each flip-flop is 50 ns. Determine the maximum operating frequency for MOD - 32 ripple counter

$$f_{max} (\text{ripple}) = 5 \times 50 \text{ ns} = 4 \text{ MHz}$$

94. What are secondary variables?

-present state variables in asynchronous sequential circuits

95. What are excitation variables?

-next state variables in asynchronous sequential circuits

96. What is fundamental mode sequential circuit?

- input variables changes if the circuit is stable
- inputs are levels, not pulses
- only one input can change at a given time

97. What are pulse mode circuit?

- inputs are pulses
- width of pulses are long for circuit to respond to the input
- pulse width must not be so long that it is still present after the new state is reached

98. What are the significance of state assignment?

In synchronous circuits-state assignments are made with the objective of circuit reduction

Asynchronous circuits-its objective is to avoid critical races

99. When do race condition occur?

-two or more binary state variables change their value in response to the change in i/p variable

100.What is non critical race?

- final stable state does not depend on the order in which the state variable changes
- race condition is not harmful

101.What is critical race?

- final stable state depends on the order in which the state variable changes
- race condition is harmful

102. When does a cycle occur?

-asynchronous circuit makes a transition through a series of unstable state

103.What are the different techniques used in state assignment?

- shared row state assignment
- one hot state assignment

104.What are the steps for the design of asynchronous sequential circuit? -construction of primitive flow table

- reduction of flow table
- state assignment is made
- realization of primitive flow table

105.What is hazard?

- unwanted switching transients

106.What is static 1 hazard?

- output goes momentarily 0 when it should remain at 1

**107. What is static 0 hazard?**

-output goes momentarily 1 when it should remain at 0

**108. What is dynamic hazard?**

-output changes 3 or more times when it changes from 1 to 0 or 0 to 1

**109. What is the cause for essential hazards?**

-unequal delays along 2 or more path from same input

**110. What is flow table?**

-state table of an synchronous sequential network

**111. What is primitive flow chart? -one**

stable state per row

**112. What is combinational circuit?**

Output depends on the given input. It has no storage element.

**113. Define merger graph.**

The merger graph is defined as follows. It contains the same number of vertices as the state table contains states. A line drawn between the two state vertices indicates each compatible state pair. If two states are incompatible no connecting line is drawn.

**114. Define closed covering**

A Set of compatibles is said to be closed if, for every compatible contained in the set, all its implied compatibles are also contained in the set. A closed set of compatibles, which contains all the states of M, is called a closed covering.

**115. Define state table.**

For the design of sequential counters we have to relate present states and next states. The table, which represents the relationship between present states and next states, is called state table.

**116. Define total state**

The combination of level signals that appear at the inputs and the outputs of the delays define what is called the total state of the circuit.

**117. What are the steps for the design of asynchronous sequential circuit?**

1. Construction of a primitive flow table from the problem statement.
2. Primitive flow table is reduced by eliminating redundant states using the state reduction
3. State assignment is made
4. The primitive flow table is realized using appropriate logic elements.

**118. Define primitive flow table :**

**It is defined as a flow table which has exactly one stable state for each row in the table. The design process begins with the construction of primitive flow table.**

**119. What are the types of asynchronous circuits ?**

- 1. Fundamental mode circuits**
- 2. Pulse mode circuits**

**120. Give the comparison between state Assignment Synchronous circuit and state assignment asynchronous circuit.**

**In synchronous circuit, the state assignments are made with the objective of circuit reduction. In asynchronous circuits, the objective of state assignment is to avoid critical races.**

**121. What are races?**

**When 2 or more binary state variables change their value in response to a change in an input variable, race condition occurs in an asynchronous sequential circuit. In case of unequal delays, a race condition may cause the state variables to change in an unpredictable manner.**

**122. Define non critical race.**

**If the final stable state that the circuit reaches does not depend on the order in which the state variable changes, the race condition is not harmful and it is called a non critical race.**

**123. Define critical race?**

**If the final stable state depends on the order in which the state variable changes, the race condition is harmful and it is called a critical race.**

**124. What is a cycle?**

**A cycle occurs when an asynchronous circuit makes a transition through a series of unstable states. If a cycle does not contain a stable state, the circuit will go from one unstable to stable to another, until the inputs are changed.**

**125. Write a short note on fundamental mode asynchronous circuit.**

**Fundamental mode circuit assumes that. The input variables change only when the circuit is stable. Only one input variable can change at a given time and inputs are levels and not pulses.**

**126. Write a short note on pulse mode circuit.**

**Pulse mode circuit assumes that the input variables are pulses instead of level. The width of the pulses is long enough for the circuit to respond to the input and the pulse width must not be so long that it is still present after the new state is reached.**

**127. Define secondary variables**

The delay elements provide a short term memory for the sequential circuit. The present state and next state variables in asynchronous sequential circuits are called secondary variables.

128. Define flow table in asynchronous sequential circuit.

In asynchronous sequential circuit state table is known as flow table because of the behaviour of the asynchronous sequential circuit. The stage changes occur independent of a clock, based on the logic propagation delay, and cause the states to flow from one to another.

129. A pulse mode asynchronous machine has two inputs. It produces an output whenever two consecutive pulses occur on one input line only. The output remains at 1 until a pulse has occurred on the other input line. Write down the state table for the machine.

Soln :

Present state	Next state		Output Z
	X	Y	
A	B	C	0
B	D	C	0
C	B	E	0
D	D	A	1
E	A	E	1

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**130. What is fundamental mode.**

A transition from one stable state to another occurs only in response to a change in the input state. After a change in one input has occurred, no other change in any input occurs until the circuit enters a stable state. Such a mode of operation is referred to as a fundamental mode.

**131. Write short note on shared row state assignment.**

Races can be avoided by making a proper binary assignment to the state variables. Here, the state variables are assigned with binary numbers in such a way that only one state variable can change at any one state transition. To accomplish this, it is necessary that states between which transitions occur be given adjacent assignments. Two binary numbers are said to be adjacent if they differ in only one variable.

**132. Write short note on one hot state assignment.**

The one hot state assignment is another method for finding a race free state assignment. In this method, only one variable is active or hot for each row in the original flow table, i.e., it requires one state variable for each row of the flow table. Additional rows are introduced to provide single variable changes between internal state transitions.

## Part – B Unit-I

- 1) Explain with neat diagrams TTL. Disadvantages of other families. Diagram of TTL Theory Working principle
2. Discuss all the characteristics of digital IC's.

**Fan out**

**P  
o  
w  
e  
r**

**d  
i  
s  
s  
i  
p  
a  
t  
i  
o  
n**

**P  
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**M  
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n

**Fan In**

Opera  
ting  
tempe  
rature  
Power  
suppl  
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requir  
ement  
s

3. Explain with neat diagram how an open collector TTL operates. Disadvantages of other families

Diagram of  
open  
collector gate  
TTL Theory  
Working principle

4. Explain the different applications of open collector TTL. Wired logic

C  
o  
m  
m  
o  
n

b  
u  
s

s  
y  
s  
t  
e

m

D  
r  
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a

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m  
p

o  
r

r  
e  
l  
a  
y

**5. Explain in detail about schottky TTL.**

**Disadvantages of other families**

**Diagram of schottky TTL**

**Theory**

**Working principle**

**Advantages**

**6.Explain with necessary diagrams MOS &**

**CMOS. PMOS**

**NMOS**

**CMOS**

**Diagrams**

**Unit-II**

**7.Design a 4-bit binary adder/subtractor circuit. Basic equations**  
Comparison of equations  
Design using twos complement Circuit diagram

**8.Design and explain a comparator to compare two identical words. Two numbers represented by  $A = A_3A_2A_1A_0$  &  $B = B_3B_2B_1B_0$  If two numbers equal  $P = A_i B_i$**   
Obtain the logic Expression .  
Obtain the logic diagram.

**9.Explain in detail the look ahead carry generator. Block diagram**  
Explanation  
Logic diagram

**Unit-III**

**10. Design a logic circuit to convert the BCD code to Excess – 3 code. Truth Table for BCD to Excess – 3 conversion.**  
K-map simplification  
Logic circuit implementing the Boolean Expression

**11.Explain in detail about PLA and PAL.**  
Logic difference between Prom & PLA  
Logic diagram implementing a function  
Logic difference between Prom & PAL  
Logic diagram implementing a function

12. Implement  $F(A,B,C,D) = (1,3,4,11,12,13,14,15)$  using multiplexer.

Implementation

Table

explanation

13. Implement  $W(A,B,C,D) = (2,12,13)$

$X(A,B,C,D) = (7,8,9,10,11,12,13,14,15)$

$Y(A,B,C,D) = (0,2,3,4,5,6,7,8,10,11,15)$

$Z(A,B,C,D) = (1,2,8,12,13)$  using PAL(16)

Table

PAL implementation

#### Unit-IV

14. Explain the working of BCD Ripple Counter with the help of state diagram and logic diagram.

BCD Ripple Counter Count  
sequence Truth Table

State diagram representing the Truth  
Table Truth Table for the J-K Flip Flop  
Logic Diagram

15. Design a sequential detector which produces an output 1 every time the input sequence 1011 is detected.

Construct state diagram  
Obtain the flow table  
Obtain the flow table & output  
table Transition table  
Select flip flop  
Excitation table  
Logic diagram

16. Explain in detail about serial in serial out shift register. Block diagram

Theoretical  
explanation Logic  
diagram Working

**Unit-V**

**17.Explain with neat diagram the different hazards and the way to eliminate them.**

**Classification of hazards**  
**Static hazard & Dynamic hazard definitions**  
**K map for selected functions**  
**Method of elimination**  
**Essential hazards**

**18.State with a neat example the method for the minimization of primitive flow table. Consider a state diagram**

**Obtain the flow table**

**Using implication table reduce the flow table**

**Using merger graph obtain maximal compatibles**

**Verify closed & covered conditions**

**Plot the reduced flow table**

**19.Design a asynchronous sequential circuit with 2 inputs T and C. The output attains a value of 1 when  $T = 1$  & c moves from 1 to 0. Otherwise the output is 0.**

**Obtain the state diagram**

**Obtain the flow table**

**Using implication table reduce the flow table**

**Using merger graph obtain maximal compatibles**

**Verify closed & covered conditions**

**Plot the reduced flow**

**table Obtain transition**

**table Excitation table**

**Logic diagram**

**20. Explain in detail about**

**Races. Basics of races**

**Problem created due to**

**races Classification of**

**races Remedy for races**

**cycles**

**21. Explain the different methods of state assignment Three row state assignment**

**Shared row state assignment**

**Four row flow table**

**Multiple row state assignment**

**Prevention of races.**

