Code No: 37138 **Set No. 1**

IV B.Tech I Semester Supplimentary Examinations, May/Jun 2009
VLSI DESIGN
(Common to Electrical & Electronic Engineering, Electronics & Instrumentation Engineering, Electronics & Control Engineering and Electronics & Computer Engineering)

Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Describe in detail metallization process in IC technogly. [16]
2. (a) Derive an equation for I_{ds} of an n channel enhancement MOSFET operating in saturation region.
   (b) An n MOS transistor is operating in saturation region with the following parameters.V_{gs}=5V, V_{tn} =1.2V, (W/L) =10: $\mu_n c_{ox}$=110μA/V^2. Find transconductance of the device. [8+8]
3. (a) what is a stick diagram? Draw the stick diagram and layout for a CMOS inverter.
   (b) What are the effects of scaling on V_t?
   (c) What are design rules? Why is metal- metal spacing larger than poly -poly spacing. [8+4+4]
4. Two nMOS inverters are cascaded to drive a capacitive load C_L=16 $\square C_g$. Calculate the pair delay (V_{in} to V_{out}) in terms of τ for the inverter geometry indicated in figure 4. What are the ratios of each inverter? If strays and wiring are allowed for,it would be reasonable to increase the capacitance to ground across the output of each inverter by 4 $\square C_g$. What is the pair delayallowing for strays? Assume a suitable value for τ and evaluate this pair delay. [16]
   Inverter 1 $L_{pu} = 16\lambda$, $W_{pu} = 2\lambda$, $L_{pd} = 2\lambda$,$W_{pd} = 2\lambda$
   Inverter 2 $L_{pu} = 2\lambda$,$W_{pu} = 2\lambda$, $L_{pd} = 2\lambda$, $W_{pd} = 8\lambda$

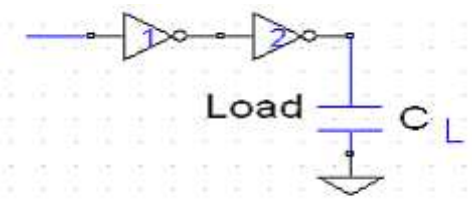

Figure 4

5. (a) Explain how the transistor might be sized to optimize the delay through the carry stage in parallel adder.
   (b) Design a two input XOR using a ROM. [8+8]
6. (a) Draw the diagram of programmed I/O pad and explain how the antifuses are used in this.

(b) Draw and explain the AND/OR representation of PLA. [8+8]

7. (a) Write a VHDL program in behavioral modeling with concurrent signal assignment.

   (b) Explain the method of switch-level simulation for CMOS circuits and name such a simulators. [8+8]

8. (a) Explain different fault models in detail.

   (b) Draw the general view of the TAP data register and explain how a boundary scan register is used for testing. [8+8]

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. With neat sketches necessary, explain the oxidation process in the IC fabrication process. [16]
2. (a) Why resistor pull up is not used in MOS circuits?
   (b) Discuss different forms of pull up, mentioning merits and demerits of each form.
   [4+12]
3. Explain the following
   (a) Double metal MOS process rules.
   (b) Design rules for P- well CMOS process. [8+8]
4. (a) Differentiate between nMOS inverter pair delay and CMOS inverter pair delay.
   (b) Derive the expressions for rise and fall time of CMOS inverter delay.
   (c) What is the total input capacitance value offered by the inverter to achieve symmetrical operation? [6+8+2]
5. Develop a model of word line decoder delay for a RAM with 2^n rows and 2^m columns. Assume true and complementary inputs are available and that the input capacitance equals the capacitance of one of the columns of H=2^m. Use static CMOS gates and express result in terms of n and m. [16]
6. (a) Draw the diagram of programmed I/O pad and explain how the antifuses are used in this.
   (b) Draw and explain the AND/OR representation of PLA. [8+8]
7. (a) What is the importance of operator precedence in VHDL? Is the AND operation takes place before OR operation?
   (b) What is mean by Hierarchy in VHDL? Write a program for 4 input multiplexer from 2 input multiplexers. [8+8]
8. (a) Explain how function of system can be tested.
   (b) Explain any one of the method of testing bridge faults.
   (c) What type of faults can be reduced by improving layout design? [6+5+5]

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Code No: 37138 **Set No. 3**

IV B.Tech I Semester Supplimentary Examinations, May/Jun 2009
VLSI DESIGN
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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. (a) Discuss fabrication differences between NMOS and CMOS technologies. Which fabrication is preferred and why?
   (b) Explain the various steps in PMOS fabrication. [8+8]
2. (a) Explain briefly about MOS transistor switch.
   (b) Discuss the square law model of FET. [8+8]
3. (a) Discuss the rule for n well and V_{DD} and V_{ss} contacts (2μm CMOS).
   (b) Discuss the rule for pad and over glass geometry (2μm CMOS). [8+8]
4. Calculate ON resistance of the circuit shown in figure 4. From V_{DD} to ground. If n channel resistance is $R_{sn} = 10^4\ \Omega$ per square. [16]

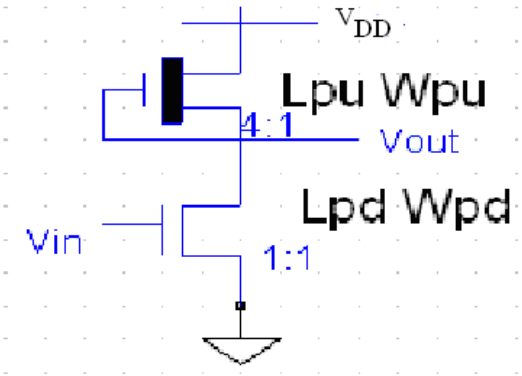

Figure 4

5. (a) Explain how the transistor might be sized to optimize the delay through the carry stage in parallel adder.
   (b) Design a two input XOR using a ROM. [8+8]
6. (a) What are the differences between a gate array chip and standard-cell chip? What benefits does each implementation style have?
   (b) Write the equations for a full adder in SOP form. Sketch a 3-input, 2- output PLA implementing this logic. [8+8]
7. (a) Compare the Concurrent signal assignments, sequential signal assignments and process statements.

(b) Why resettable registers are preferable and what is the difference between Synchronous and Asynchronous resets? [8+8]

8. (a) Why the chip testing is needed? At what levels testing a chip can occur?

(b) What is the drawback of serial scan ? How to overcome this?

(c) What is the percentage fault coverage? How it is calculated? [6+4+6]

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Code No: 37138 **Set No. 4**

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Time: 3 hours **Max Marks: 80**

Answer any FIVE Questions
All Questions carry equal marks

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1. Distinguish between thin film resistors and thin film capacitors in all aspects. [16]
2. (a) Derive an equation for I_{ds} of an n channel enhancement MOSFET operating in saturation region.
   (b) An n MOS transistor is operating in saturation region with the following parameters.V_{gs}=5V, V_{tn} =1.2V, (W/L) =10: $\mu_n c_{ox}$=110μA/V^2. Find transconductance of the device. [8+8]
3. (a) Discuss the rule for n well and V_{DD} and V_{ss} contacts (2μm CMOS).
   (b) Discuss the rule for pad and over glass geometry (2μm CMOS). [8+8]
4. Calculate on resistance of the circuit shown in the figure 4 from V_{DD} to GND. If n- channel sheet resistance R_{sn}=10^4 Ω per square and P-channel sheet resistance $R_{sp} = 3.5 \times 10^4$ Ω per square. [16]

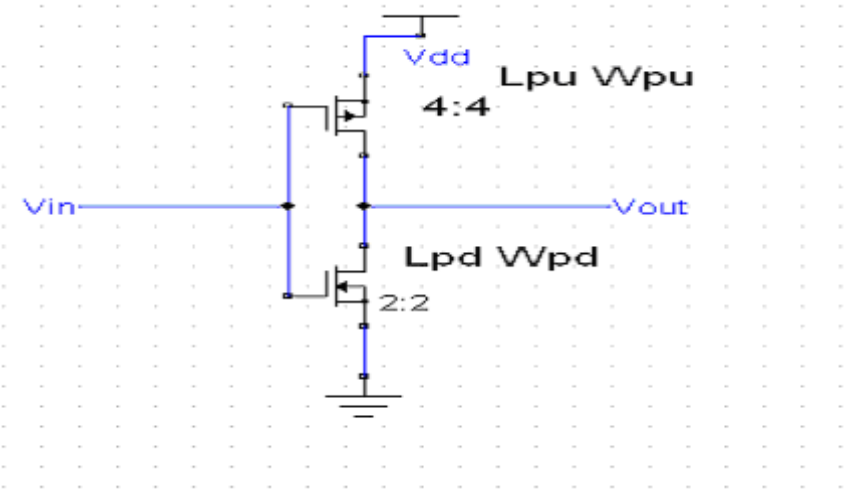

Figure 4

5. Draw the logic diagram for a ripple-carry binary counter using T registers and explain its operation with the help of truth table and also compare it with synchronous counters. Draw the schematic for T register. [16]
6. (a) Draw the typical architecture of PAL and explain the operation of it.
   (b) What is CPLD? Draw its basic structure and give its applications. [8+8]

7. (a) Explain how a FSM model is described in VHDL with suitable program.
   (b) What is the difference between Design capture tools and design verification tools? Give some examples of each. [8+8]

8. (a) Explain the gate level and function level of testing.
   (b) A sequential circuit with in? inputs and 'm' storage devices. To test this circuit how many test vectors are required.
   (c) What is sequential fault grading? Explain how it is analyzed. [6+4+6]

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