

IV B.Tech I Semester Examinations, May 2011

VLSI DESIGN

Common to Electronics And Computer Engineering, Electronics And Control Engineering, Electronics And Instrumentation Engineering, Electrical And Electronics Engineering

Time: 3 hours

Max Marks: 80

Answer any FIVE Questions
All Questions carry equal marks

1. (a) Explain the structure of MOS enhancement mode, Depletion mode and PMOS enhancement mode transistors.
(b) Explain the working of an enhancement mode transistor with suitable diagrams. [12+4]
2. (a) What is BIST? Explain in detail.
(b) Write the advantages of BIST. [10+6]
3. (a) Draw a self timed dynamic PLA and what are the advantages of it compared to footed dynamic PLA.
(b) Explain the tradeoffs between using a transmission gate or a tristate buffer to implement an FPGA routing block. [8+8]
4. Briefly discuss the limits of scaling. Why scaling is necessary for VLSI circuits? [16]
5. (a) Compare the Hardware and Software Languages.
(b) Draw the basic design flow through typical CMOS VLSI tools and give some names of corresponding tools. [8+8]
6. (a) Explain how a Booth recoded multiplier reduces the number of adders.
(b) Draw circuit diagram of a one transistor with transistor capacitor dynamic RAM and also draw its layout. [8+8]
7. Design a two-input OR gate in domino logic and pseudo nMOS logic and Pseudo nMOS logic by
(a) Drawing a transistor schematic.
(b) Explaining its operation. [8+8]
8. A CMOS process produces gate oxides with a thickness of $t_{ox} = 100\text{\AA}$. The FET carriers mobility values are given as $\mu_n = 550\text{cm}^2/\text{V}\cdot\text{Sec}$, $\mu_p = 210\text{cm}^2/\text{V}\cdot\text{Sec}$.
(a) Calculate the oxide capacitance per unit area in units of $\text{pF}/\mu\text{m}^2$.
(b) Find the process transconductance values for nFET and pFET. Place your answer in units of $\mu\text{A}/\text{V}^2$. [16]

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