

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
IV B.TECH – I SEM SUPPLEMENTARY EXAMINATIONS, JUNE – 2010
VLSI SYSTEM DESIGN
(COMMON TO CSE, CSS, ECC)

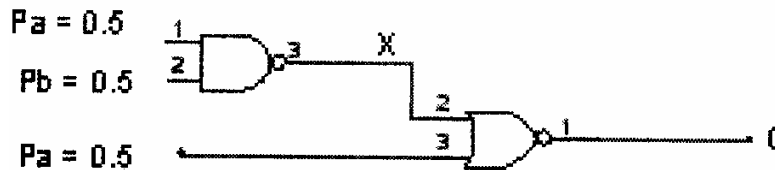
Time: 3hours

Max.Marks:80

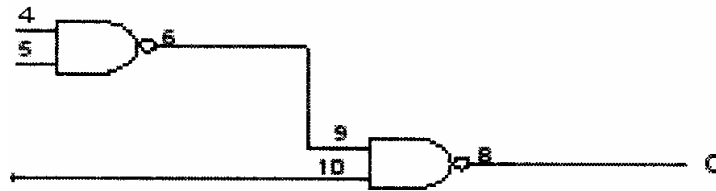
Answer any FIVE questions
All questions carry equal marks

- - -

1. Implement the following gates with n-MOS transistors only and explain its working:
 - a) 2 Input OR gate
 - b) 4 Input NAND gate. [8+8]
- 2.a) Define Moore's Law.
- b) Why ICs are more reliable, accurate & faster than discrete devices? [8+8]
3. Design a stick diagram in CMOS logic for the function given below.
 $Y = \{(A+B+C) D\}$ [16]
4. Design a layout for NMOS 3-input NOR gate. [16]
- 5.a) Compute the Zero delay signal probabilities for all signals for the network shown in figure.



- b) Find the combination of input transitions which introduces maximum of glitching at the primary output '0' assuming that all gates have a delay of one unit time shown in figure. [8+8]



6. Draw the Architecture of PLA and explain how different logic functions can be implemented using PLA. [16]
7. Explain how Architecture driven voltage scaling technique reduces the power consumption of the design. [16]
8. With suitable example explain clearly about Hardware/Software Co-simulation & Co-synthesis. [16]

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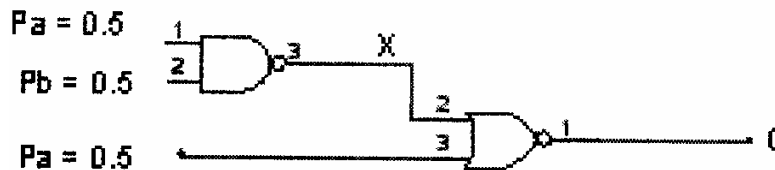
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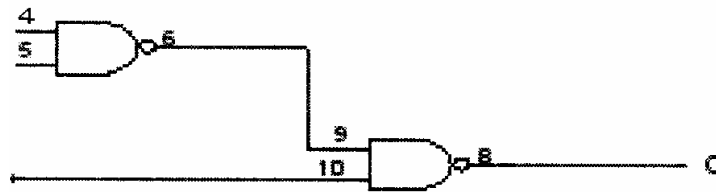
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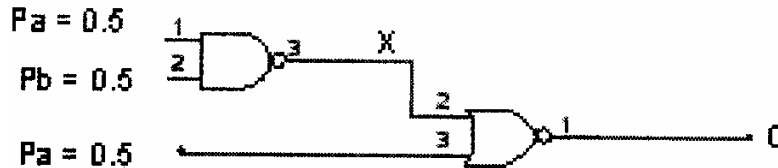
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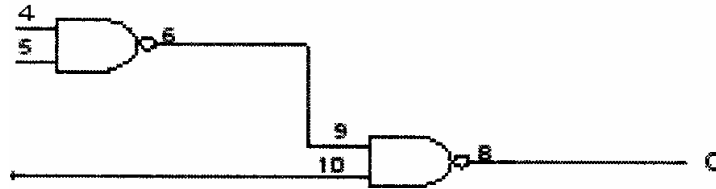
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