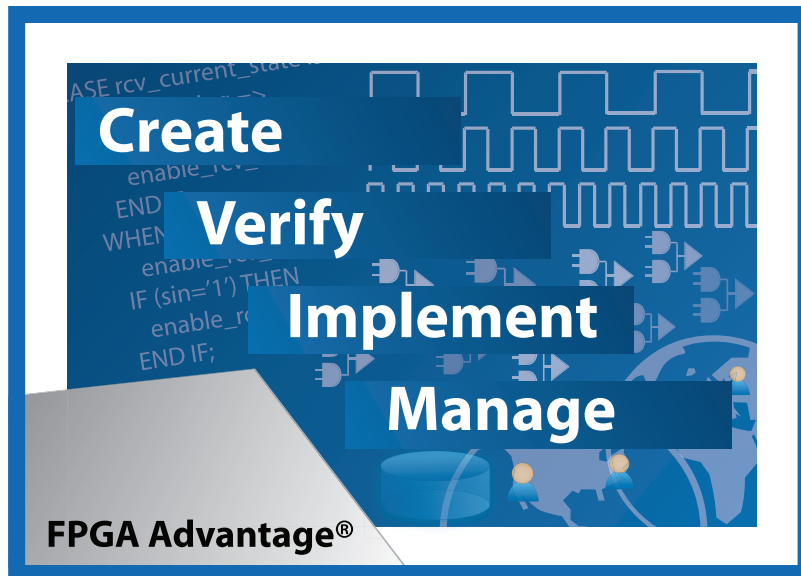


FPGA Advantage



FPGA Advantage continually meets the challenges of complex FPGA architectures by providing advanced technologies to optimize creation, verification, implementation, and design management.

Key Product Benefits

- Integrated, vendor-independent design environment supporting all FPGA families
- Comprehensive, HDL-based FPGA design flow uniting HDL Designer Series, Precision Synthesis and ModelSim
- Rapid design creation and reuse through visualization, analysis, and verification woven throughout the complete design flow
- Architecture-aware implementation for all popular FPGA families

FPGA Advantage

Providing the industry's only comprehensive vendor-independent FPGA design flow, Mentor Graphics FPGA Advantage® integrates the proven capabilities of HDL Designer Series™ for design analysis, reuse, creation and management; ModelSim for verification; and Precision® Synthesis for advanced device implementation. FPGA Advantage delivers the power and capacity necessary for today's complex FPGA designs.

Create

HDL Designer Series assists engineers in creating new functionality, analyzing, assessing, and visualizing existing complex RTL designs for reuse as part of the new design. HDL Designer Series provides tools enabling code integrity analysis, connectivity completeness analysis, HDL code quality assessment, and design visualization. In addition to advanced editors needed to create the design, HDL Designer Series includes the innovative Interface-Based Design (IBD) editor that displays HDL code and block diagrams as a spreadsheet describing the connectivity between design blocks. Engineers can dynamically view the design to show either the signals and connectivity across levels of hierarchy or a traditional block diagram.

Instead of relying on a subjective analysis of how good the project code is, HDL Designer Series analyzes code based on a selected design rule set. Detailed scoring metrics associated with these design rule sets provide an overall quality score, enabling engineers to identify potential problem areas as they design, as well as the ability to provide management with an objective, detailed analysis — allowing design groups to understand where more work is needed.

Included in HDL Designer Series are customizable data management and analysis capabilities, enabling designers to selectively view, search, organize, and correlate design data — all improving the productivity of each individual engineer.

Every product design requires design documentation without which, design information cannot be communicated, making product support difficult and future design reuse almost impossible. HDL Designer Series supports automated documentation, leveraging Microsoft® Object Linking and Embedding (OLE) and HTML export — enabling designers to document while they design.

Verify

ModelSim® simulation combines high performance and capacity with the most advanced code coverage and debugging capabilities in the industry, offering unmatched flexibility. Model Technology™ was the first to put the award-winning single-kernel simulator (SKS) technology in the hands of engineers, enabling the transparent mixing of VHDL, Verilog, and SystemC in one design, through a common, intuitive graphical interface for development and debug at any level, regardless of the language.

An intelligently engineered GUI makes efficient use of desktop real estate, allowing designers to easily customize it to their preferences. The GUI's organizational and filtering capabilities help to focus on serious potential problems or on the causes of simulation failures.

Many ModelSim debug and analysis capabilities may be employed post-simulation on saved results as well as during live simulation runs. For example, the coverage viewer will analyze and annotate source with code coverage results, including FSM state and transition, statement, expression, branch, and toggle coverage.

ModelSim advanced code coverage capabilities are integrated into the tool. Integrated code coverage provides the highest performance with the greatest ease of use. ModelSim coverage metrics provide instance-based results for all supported metric types. All coverage information is now stored in the Unified Coverage Database (UCDB). The UCDB is used to collect and manage all coverage information in one highly efficient database. Coverage utilities that analyze code coverage data, such as merging and test ranking, are available. A coverage viewer eliminates the need to load and have active a simulation in order to review code coverage results.

The combination of industry-leading performance and capacity with the best integrated debug and analysis environment make ModelSim the simulator of choice for FPGA design.

Implement

FPGA designs have become increasingly challenging, requiring incremental design methodologies to effectively manage complexity, reduce risk and accelerate time to market. Moreover, designers must fine-tune FPGA implementations to ensure that their challenging designs meet technical and business requirements. Precision physically aware synthesis allows designers to maximize their results while minimizing effort.

With advanced support for ASIC prototyping (support for DesignWare® libraries, SDC constraints, gated-clock handling, etc.) plus advanced implementation and optimization techniques such as automatic mapping and inferencing of dedicated DSP and RAM blocks, Precision Synthesis is uniquely suited to handle today's high-end FPGAs. In addition, Precision Synthesis features an award-winning design analysis capability, allowing designers to cross-probe between multiple views as well as perform interactive static timing for rapid "what-if" analyses. Precision Synthesis reduces design iterations, and enables faster, more predictable completion of designs, while delivering high quality of results (QoR).

Integration

HDL Designer Series, ModelSim, and Precision synthesis accelerate the FPGA design process by providing unique tool integration. Built into each of the tools is the ability to communicate design information to rapidly initiate downstream processes or identify problematic results back to the source — all with a click of a mouse. The HDL Designer Series integration with ModelSim allows for simple point-and-click start to verification, eliminating time-consuming manual steps to begin the process. Cross control/probing between HDL Designer Series and ModelSim enables integration of the verification and design process, thus decreasing the time to isolate and fix problems that arise. The same type of integration exists between HDL Designer Series and Precision synthesis. HDL Designer enables a simple point-and-click start to the implementation process, eliminating the time and effort of manual start up. Synthesized results can be cross probed back to the source design within HDL Designer Series, enabling rapid design iterations and reducing overall design cycle time.

Bringing it All Together

FPGA Advantage is the centerpiece of the comprehensive Mentor Graphics FPGA design flow, bringing together the design management and creation capabilities of HDL Designer Series, the performance and capacity of ModelSim simulation, and the advance implementation and optimization techniques of Precision Synthesis. From electronic system-level (ESL) design, design creation management, and logic synthesis to simulation, FPGA-PCB integration, and PCB design, Mentor Graphics supports the complete design flow.

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