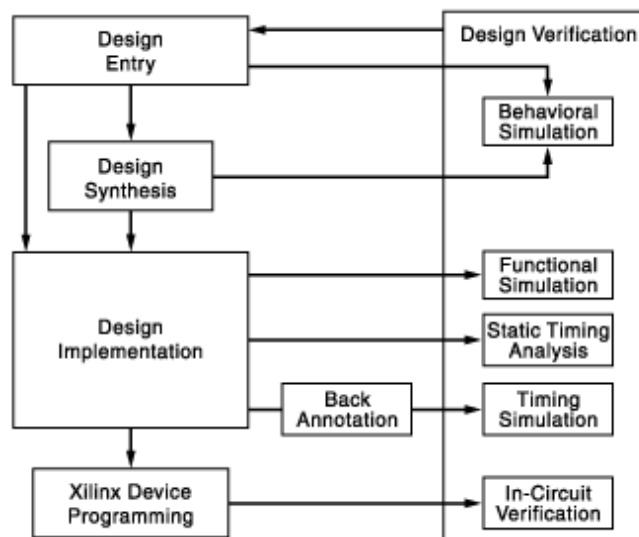


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FPGA Design Flow Overview

The ISE™ design flow comprises the following steps: design entry, design synthesis, design implementation, and Xilinx® device programming. Design verification, which includes both functional verification and timing verification, takes places at different points during the design flow. This section describes what to do during each step. For additional details on each design step, click a box in the following figure.



Design Entry

Create an ISE project as follows:

1. Create a project. [HOW?](#)
2. Create files and add them to your project, including a user constraints (UCF) file. [HOW?](#)
3. Add any existing files to your project. [HOW?](#)
4. Assign constraints such as timing constraints, pin assignments, and area constraints. [HOW?](#)

Functional Verification

You can verify the functionality of your design at different points in the design flow as follows:

- Before synthesis, run behavioral simulation (also known as RTL simulation). [HOW?](#)
- After Translate, run functional simulation (also known as gate-level simulation), using the SIMPRIM library. [HOW?](#)
- After device programming, run in-circuit verification. [HOW?](#)

Design Synthesis

Synthesize your design. [HOW?](#)

Design Implementation

Implement your design as follows:

1. Implement your design, which includes the following steps: **HOW?**
 - Translate
 - Map
 - Place and Route
2. Review reports generated by the Implement Design process, such as the Map Report or Place & Route Report, and change any of the following to improve your design:
 - Process properties **HOW?**
 - Constraints **HOW?**
 - Source files **HOW?**
3. Synthesize and implement your design again until design requirements are met.

Timing Verification

You can verify the timing of your design at different points in the design flow as follows:

- Run static timing analysis at the following points in the design flow:
 - After Map **HOW?**
 - After Place & Route **HOW?**
- Run timing simulation at the following points in the design flow:
 - After Map (for a partial timing analysis of CLB and IOB delays) **HOW?**
 - After Place and Route (for full timing analysis of block and net delays) **HOW?**

Xilinx Device Programming

Program your Xilinx device as follows:

1. Create a programming file (BIT) to program your FPGA. **HOW?**
2. Generate a PROM, ACE, or JTAG file for debugging or to download to your device. **HOW?**
3. Use iMPACT to program the device with a programming cable. **HOW?**

See Also

[FPGA Advanced Flows](#)

[FPGA Basic Flow](#)

Send any feedback on this topic to isedocs@xilinx.com.
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